REMARKS/ARGUMENTS

The present application is a continuation of U.S. Patent Application Serial No. 09/651,948. In the parent application, the examiner issued an office action (dated May 29, 2003) rejecting some claims and indicating that other claims were allowable. The applicants accepted the allowable claims to expedite issuance of a patent. The following arguments are made to obviate similar rejections from the examiner.

Status of the Claims

Claims 1-24 were originally filed in the parent application. Claims 10-12 and 16-18 were indicated to be allowable in the parent and are canceled here. Accordingly, claims 1-9, 13-15, and 19-24 are pending.

Independent claims 13, 19 and 24 have been amended to clarify the claim wording.

Objections to the Specification

The examiner objected to the original specification as missing serial numbers on pages 1-3. The foregoing amendments provide the missing serial numbers.

The examiner further objected to the original specification as using the term "ways" in a manner that is not consistent with how the term is used in the art. Applicants respectfully disagree. The term "way" is used consistently with the usage in the art concerning N-way set associative caches, in which a cache is divided into N different sets or "ways" containing multiple cache lines. Each way is associated with a corresponding portion of main memory, and each of the cache lines within each way can store data from any position within the associated portion of main memory.

The specification notes that a way is segmented across a number of banks. See, e.g., the original specification page 6, lines 1-2 and page 8, lines 10-11. Thus, e.g., each bank could have, say, thirty-two cache lines from each way. Thus, ways and banks are not synonymous as the examiner suggests. The examiner is invited to call the undersigned if further discussion might be helpful in resolving this point.

Rejections under 35 U.S.C. § 103

Claims 1-2, 7-9, 13-15, 19, and 21-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,055,204 ("Bosshart"). Claims 3-6 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bosshart in view of U.S. Patent No. 6,351,797 ("Beard"). Applicants respectfully traverse because the examiner has not established a prima facie case of obviousness.

To make a rejection under § 103, the examiner must establish a prima facie case of obviousness. *See* MPEP 2142.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Id (emphasis added). Applicants assert that the cited art does not teach or suggest all the claim limitations.

For example, independent claim 1 recites in part:

> a set associative cache having a plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way has a fast access time; [and]
> access control logic ... to remap any defective way in a bank to the first way in that same bank.

The examiner cites Bosshart at Fig. 8a (elements 100T0-3) and column 17, lines 7-54) as teaching that the fast way is used as the spare because it "is physically closer to the access control logic." Page 4. However, there are a number of faults with this assertion. First, Bossart uses the term "way" in the same conceptual manner as the applicants, and Bosshart nowhere teaches or suggests that elements 100T0-3 represent a way. Rather, it is a group of spare rows that may be used individually or as a block to replace defective rows. When used as a block, Bosshart notes each way has a corresponding row in the block. *See* col. 20, lines 20-38. Second, Bosshart at col. 17, lines 35-58, describes the configuration of each of the banks as having a top half and a bottom half

"separated by a sense amplifier line [which] may be energized to read information from a given way of either the top half or bottom half." Thus the ways that are more proximate the center (the sense amplifier line) would be the faster ways. Finally, Bossart notes at col. 3, lines 31-36, that Fig. 8a is a block diagram (as opposed to other figures which present electrical diagrams). Given that Fig. 8a is a block diagram, particularly in view of the manner in which memory 92 is presented, no inference can be drawn that elements 100T0-3 is in fact physically closer to the access control logic. To emphasize this final point, applicants note that element 100B0-3 play the same role as elements 100T0-3, and yet they are drawn on the opposite side of memory 92.

Applicants can find no teaching or suggestion of the above-cited claim limitations in either Bossart or Beard. Accordingly, applicants assert that independent claim 1 and its dependent claims 2-9 are allowable over the cited art for at least this reason.

As amended, independent claim 13 recites in part: "a set associative cache having a plurality of ways that are each segmented into a plurality of banks ... wherein each bank includes a first way that has a physically shorter path to said access control logic; and ... wherein the access control logic controls the mux in a given bank to remap any defective way in that bank to the first way in that same bank." Independent claim 24 recites similar limitations. To anticipate these limitations, the examiner relies on the same reasoning applied in rejecting claim 1. Applicants assert that the cited art fails to teach or suggest these claim limitations for the same reasons argued above. Accordingly, independent claim 13, its dependent claims 14-15, and independent claim 24, are allowable over the cited art for at least this reason.

As amended, independent claim 19 recites in part: "providing a set associative cache with a plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way in each bank has a fastest access time; ... and using the mux in a bank to remap any defective way in a bank to the first way in that same bank." To anticipate these limitations, the examiner relies on the same reasoning applied in rejecting claim 1. Applicants assert that the cited art fails to teach or suggest these claim limitations for the same reasons argued

above. Accordingly, independent claim 19 and its dependent claims 20-23 are allowable over the cited art for at least this reason.

Conclusion

In the course of the foregoing discussions, applicant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

In view of the foregoing amendments and remarks, applicant submits that all pending claims are now in condition for allowance, and an early notice to that effect is earnestly solicited. If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

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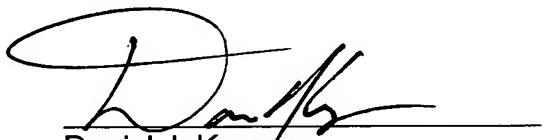
Respectfully submitted,



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